

VME-IFoIP-WB



IN-SNEC®

VME IF over IP Wideband Acquisition boards

The VME-IFoIP (Intermediate Frequency over Ethernet Protocol) family is composed of the following VME 6U form factor boards :

- VME-IFoIP-WB
- VME-IFoIP-SPC
- VME-IFoIP-HPC

The input signal is wideband digitized with an adjustable sampling frequency, channelized, formatted, optionally processed in FPGAs. Sample flows are then routed to computer nodes over one or several LANs, using the Gigabit Ethernet interfaces.

Together with the wideband acquisition board comes an easy to use library to help the users to develop their own applications.

VME-IFoIP-WB - Wideband Acquisition board

The VME-IFoIP-WB wideband acquisition board is composed of two boards : a MADBA acquisition daughter board and a VME Gateway board, integrated in a VME 6U form factor within 2 slots.

This system features 4 RF analog inputs, 32 DDC, 4 Virtex-II FPGA, 4 Gigabit Ethernet.

The input signal is wideband digitized with a sampling frequency up to 105 MHz, with ability of under-sampling.

Software is delivered with the OS QNX Momentics 6.3.

VME-IFoIP-SPC - Standard Processing Capability Acquisition board

The VME-IFoIP-SPC wideband acquisition board is composed of one daughter board mounted on a Standard Processing Capacity mother board integrated in a VME 6U form factor within 1 slot.

This system features 2 RF analog inputs in either 70 MHz or 140 MHz intermediate frequency or L Band, 8 DDC, 1 Virtex-V FPGA FX100T, 4 Gigabit Ethernet.

The input signal is wideband digitized with a sampling frequency up to 186 MHz

VME-IFoIP-HPC - High Processing Capability Acquisition board

The VME-IFoIP-HPC wideband acquisition board is composed of one daughter board mounted on a High Processing Capacity mother board integrated in a VME 6U form factor within 1 slot.

This system features 2 RF analog inputs in either 70 MHz or 140 MHz intermediate frequency or L Band, up to 32 DDC, 1 Virtex-V FPGA SX240T, 4 Gigabit Ethernet.

The input signal is wideband digitized with a sampling frequency up to 186 MHz.

Applications

- Digital communications
- Base stations
- Modems
- SDR products

Main Features

- High speed digitizer
- 32 DDC up to 2.5MHz bandwidth
- Architecture based on programmable FPGA
- Ethernet plug and play board

Main Benefits

- Open and evolutive architecture
- Standard interfaces

Options

- IF=70MHz
- User configuration
- Filtering
- FFT

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Modele references

| | |
|-------------------------|--|
| VME-IFoIP-WB-x-y-z | x = 140 or 70 MHz y = N inputs (4 by default) z = Virtex-II 3000 gates |
| VME-IFoIP-WB-140-4-3000 | SM01005305 C |
| VME-IFoIP-WB-70-4-3000 | SM01005305 E |

Technical characteristics

Channelization

| | |
|-------------------|---|
| Technique | Digital Down Converter |
| Implementation | 8 GC401 6 |
| Channels quantity | 32 |
| Output frequency | Independent for each narrowband channel Efficient transfer to the DSP (blocks- without tagging) |
| WB channelizing | F _s = 2.5 MHz with F _e = 80MHz |

Pre-processing (FPGA)

| | |
|---------------------------|-----------------------------|
| Number and type of FPGA | |
| MADBA board | 2 XILINX Virtex-II 3M gates |
| Gateway board | 2 XILINX Virtex-II 2M gates |
| ADC + DDC synchronization | Yes (internal / external) |
| Datation | Yes |
| User configuration | Option |
| Filtering | Option |
| FFT | Option |
| Sampling | ADC output / DDC output |

Processor

| | |
|-----------|--------------------------|
| Type | 2 x MPC 8560 |
| Computing | 1850 MIPS each processor |
| Flash | 2x 4M x 32 |
| RAM | 2x 16M x 64 |
| FIFO | 4 FIFO 256K x 32 bits |

Data transfer

| | |
|---------------------------|--|
| Mode | Data flow de-interleaving |
| Implementation | 4 Gigabits Ethernet ports |
| Control | Protocol TCP/IP |
| Data ports quantity | 1 port per data flow (from 1 to 32) |
| Clients quantity | 1 client per narrowband flow (from 1 to 32) |
| Monitoring ports quantity | 4 (1 per HSI) |

Digital interfaces

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|---------------------|-----|
| FPDP | Yes |
| GPIO (synchro, etc) | Yes |

Mechanical characteristics

| | |
|------------|---|
| Dimensions | 9"2x6"3x3/4" (233x160x19mm) VME form factor (6Ux2 slots) |
|------------|---|

Interfaces

| | |
|--------------|------------------------------|
| RF inputs | 4 SMA female |
| 10 MHz input | SMA female |
| GPIO | 26 pins M [1/2"] (1.27mm) |
| FPDP | 50 pins M [1/2"] (1.27mm) |
| VME | P1,P2 |
| Ethernet | 4 connectors RJ45 1000 baseT |

Software

| | |
|------------------|--------------------------|
| C source drivers | yes |
| OS | QNX Momentics 6.3, Linux |

VME-IFoIP-WB

Description

Input path and analog to digital conversion

Each of the 4 inputs is analog-conditionned by a scalable gain in order to fit the ADC maximum resolution. The signal can be directly base-band digitized without filtering, but under-sampling is also possible, since the board features 34 MHz SAW filters centered on 140 MHz or 70 MHz (option value to be indicated when ordering) in order to remove aliasing.

The 4 RF signals are digitized with the same clock. This clock is generated with an internal synthesizer designed to adjust the sampling frequency to the value needed for a signal processing application. Typically, a multiple of the modulation rates to be considered is used.

These points make the insertion of MADBA in an acquisition chain extremely simple and cost effective: it becomes possible to avoid the use of external IF to baseband converters and external clock synthesizer.

Channelization

MADBA features 32 configurable DDC that can select a sub-band among the 4 wideband sources, using 8 GC4016 Asics. Channelization stage can be by-passed to provide a direct and under-sampled access to the ADC output samples.

Pre-processing in FPGA

The basic functions of FPGA are to interface with the processor board, to control the resources and to collect the data streams. MADBA offers synchronization and datation functionalities allowing time-stamping/re-stamping of narrowband streams on one or several acquisition boards.

The board provides wideband pre-processing functionalities like the measure of the maximum value, the estimation of energy... This is done in order to allow the user for controlling the scale of the analog signal and taking advantage of the full ADC resolution.

The 4 VIRTEx-II FPGA can also support optional pre-processing functions (FFT for example) and end-user specific functions.

Processing in Powerquicc III

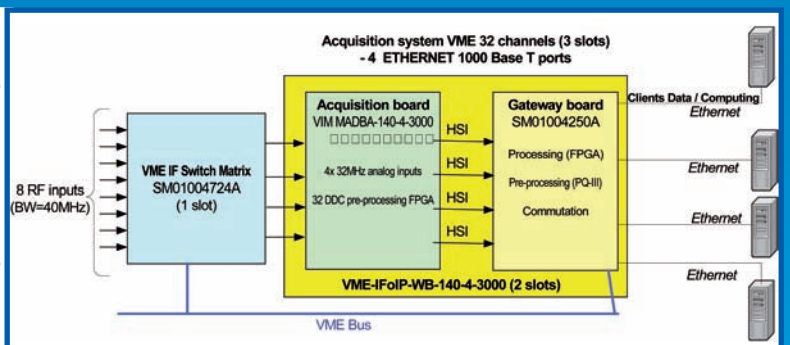
The user can take advantage of the powerful dual Powerquicc III processor associated with the open environment (QNX) to design and easily load its own processing applications.

Control and Broadcasting via TCP

Output samples are shortly bufferized and then transmitted over 4 different Gigabit Ethernet interfaces under TCP/IP protocol. Each HSI node features a Gigabit output that is managed in a multi-port way. The Gateway board hence features a real function of routing the data flows towards a network of computer nodes.

Up to 32 servers can be linked to the 32 DDC of a MADBA acquisition system with the management scheme described above.

Acquisition example



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